Serial No. 09/985,766 Docket No.: 1448.1017

IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 2, 4, 7, 8, 9, and 11 in accordance with the following:

1. (CURRENTLY AMENDED) A processor comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal ~~and which do~~ not ~~overlap~~ overlapping with said first initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed; and

a second flag that is cleared by an input of either of the first ~~or~~ and second reset signals and that is set when initial setting of the second initial setting area has been completed, wherein:

~~when either one of the first and second reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first and second initial setting areas~~

when the first reset signal is input, the first input setting area is initialized after confirmation that the first red flag is cleared and the second initial setting area is initialized after confirmation that the first flag is set and the second flag is cleared, and

when the second reset signal is input, the second initial setting area is initialized after confirmation that the first flag is set and the second flag is cleared without clearing the first flag.

2. (CURRENTLY AMENDED) The processor according to claim 1, further comprising:

a third initial setting area which is initialized based on an input of the first or second reset signals or a third input signal and which do not overlap with both said first initial setting area and said second initial setting area; and

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a third flag that is cleared by an input of any one of the first through third reset signals and that is set when initial setting of the third initial setting area has been completed, wherein:

~~when any one of the first through third reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first through third initial setting areas~~

when any one of the first and second rest signals is input, the third initial setting area is initialized after confirmation that the first and second flags are set and the third flag is cleared, and

when the third reset signal is input, the third setting area is initialized after confirmation that the first and second flags are set and the third flag is cleared without clearing the first and second flags.

3. (CURRENTLY AMENDED) The processor according to claim 2, wherein:

the first initial setting area is formed by a first register group ~~for~~ performing communication between the processor and an outside of the processor;

the third initial setting area is formed by a second register group relating to execution of instructions inside the processor; and

the second initial setting area is an area other than both the first register group and the second register group.

4. (CURRENTLY AMENDED) The processor according to claim 2, further comprising:

an n-th initial setting area, where n is an integer having a value equal to or ~~more~~ greater than 4, which ~~do~~ does not overlap with each initial setting area from the first initial setting area through an (n-1)-th initial setting area and which is initialized based on an input of the first reset signal through an n-th reset signal, different from any of the first through ~~an~~ (n-1)-th reset signals; and

an n-th flag that is cleared by an input of any of the first reset signal through the n-th reset signal and that is set when initial setting of the n-th initial setting area has been completed, wherein:

~~when any one of the first through n-th reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first through n-th initial setting areas~~

when any one of the first, second and third rest signals is input, the n-th initial setting area is initialized after confirmation that the first flag through an (n-1)-th flag

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are set and the n-th flag is cleared, and

when the n-th reset signal is input, the n-th initial setting area is initialized after confirmation that the first through (n-1)-th flags are set and the n-th flag is cleared without clearing the first through (n-1)-th flags.

5. (CURRENTLY AMENDED) The processor according to claim 1, wherein ~~the processor is provided with~~ an external input terminal ~~for receiving~~ of the processor receives the respective reset signals from the outside.

6. (ORIGINAL) The processor according to claim 1, wherein the respective reset signals are generated within the processor.

7. (CURRENTLY AMENDED) A method of controlling resetting of a processor, the processor ~~including~~comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal ~~and which do~~ not ~~overlap~~ overlapping with said first initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed; and

a second flag that is cleared by an input of either of the first ~~or~~ and second reset signals and that is set when initial setting of the second initial setting area has been completed, wherein;

~~when either one of the first and second reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first and second initial setting areas,~~

when the first reset signal is input, the first initial setting area is initialized after confirmation that the first flag is cleared and the second initial setting area is initialized after it is confirmed that the first flag is set and the second flag is cleared, and

when the second reset signal is input, the second initial setting area is initialized after confirmation that the first is set and the second flag is cleared without clearing the first flag,

the method comprising:

~~the step in which flags that correspond to each reset signal type are cleared;~~

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clearing each of the first and second flags corresponding to each of the first and second signals;

~~the step in which a state of each flag is confirmed, initial setting is performed for an initial setting area corresponding to the cleared flags and, after the initial setting is completed, setting corresponding flags is repeatedly performed until all of the flags are placed in a set state~~

confirming that each of the first and second flags is cleared, and initializing each of the first and second initial setting areas corresponding to each of the first and second flags that is cleared; and

setting each of the first and second flags repeatedly, after completion of initializing each of the first and second initial setting areas, until all of the first and second flags are set.

8. (CURRENTLY AMENDED) A method of controlling resetting of a processor, the processor ~~including~~comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal ~~and which do~~ not ~~overlap~~ overlapping with said first initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed; and

a second flag that is cleared by an input of either of the first ~~or~~ and second reset signals and that is set when initial setting of the second initial setting area has been completed, wherein:

~~when either one of the first and second reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first and second initial setting areas,~~

the method ~~comprising the steps of~~comprises:

clearing the ~~first flag~~ first and second flags ~~if~~ when the first reset signal is ~~received~~ input, and clearing the ~~first and~~ second ~~flags~~ flag ~~if~~ when the second reset signal is ~~received~~ input;

~~checking which flag/s has/have been cleared out of the first and second flags;~~

~~initializing initial setting area/s corresponding to the cleared flag/s out of the first and second areas, and~~

when the first signal is input, initializing the first initial setting area after confirming that the first flag is cleared, and initializing the second initial setting area after confirming that the

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first flag is set and the second flag is cleared;

when the second rest signal is input, initializing the second initial setting area after confirming that the first flag is set and the second flag is cleared, without clearing the first flag; and

~~setting flag/s corresponding to the initial setting area/s which has/have been initialized out of the first and second areas~~

setting each of the first and second flags corresponding to each of the first and second initial setting area which initialized.

9. (CURRENTLY AMENDED) A method of controlling resetting of a processor, the processor ~~including~~comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal ~~and which do~~ not ~~overlap~~ overlapping with said first initial setting area;

a third initial setting area which is initialized based on an input of the first or second reset signals or a third input signal ~~and which do~~ not ~~overlap~~ overlapping ~~with~~ both said first initial setting area and said second initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed;

a second flag that is cleared by an input of either of the first ~~or~~ and second reset signals and that is set when initial setting of the second initial setting area has been completed~~,~~; and

a third flag that is cleared by an input of any one of the first through third reset signals and that is set when initial setting of the third initial setting area has been completed, wherein:

~~when any one of the first through third reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first through third initial setting areas,~~

the method ~~comprising the steps of~~comprises:

clearing the ~~first flag~~ first flag to the third flag ~~if~~ when the first reset signal is ~~received~~ input, clearing the ~~first and~~ second and third flags ~~if~~ when the second reset signal is ~~received~~ input, and clearing the ~~first through~~ third ~~flags~~ flag ~~if~~ when the third reset signal is

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~~received~~ input;

~~checking which flag/s has/have been cleared out of the first through third flags;~~

~~initializing initial setting area/s corresponding to the cleared flag/s out of the first through third areas, and~~

when the first signal is input, initializing the first signal initial setting area after confirming that the first flag is cleared, initializing the second signal initial setting area after confirming that the first flag is set and the second flag is cleared, and initializing the third signal initial setting area after confirming that the first and second flags are set and the third flag is cleared;

when the second signal is input, initializing the second signal initial setting area after confirming that the first flag is set and the second flag is cleared without clearing the first flag, and initializing the third signal initial setting area after confirming that the first and second flags are set and the third flag is cleared;

when the third signal is input, initializing the third initial setting area after confirming that the first and second flags are set and the third flag is cleared without clearing the first and second flags; and

~~setting flag/s corresponding to the initial setting area/s which has/have been initialized out of the first through third areas~~

setting each of the first, second, and third flags corresponding to each of the first, second, and third initial setting area which is initialized.

10. (CURRENTLY AMENDED) The method of controlling resetting of a processor according to claim 9, wherein:

the first initial setting area is formed by a first register group ~~for~~ performing communication between the processor and an outside of the processor~~,~~;

the third initial setting area is formed by a second register group relating to the execution of instructions inside the processor~~,~~; and

the second initial setting area is an area other than both the first register group and the second register group.

11. (CURRENTLY AMENDED) A method of controlling resetting of a processor, the processor ~~including~~comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

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a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal ~~and which do~~ not ~~overlap~~ overlapping with said first initial setting area;

a third initial setting area which is initialized based on an input of the first or second reset signals or a third input signal ~~and which do~~ not ~~overlap~~ overlapping ~~with~~ both said first initial setting area and said second initial setting area;

an n-th initial setting area, where n is an integer having a value equal to or ~~more~~ greater than 4, which do not overlap with each initial setting area, from the first initial setting area through an (n-1)-th initial setting area, and which is initialized based on an input of the first reset signal through an n-th reset signal different from any of the first through ~~an~~ (n-1)-th reset signals;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed;

a second flag that is cleared by an input of either of the first ~~or~~ and second reset signals and that is set when initial setting of the second initial setting area has been completed;

a third flag that is cleared by an input of any one of the first through third reset signals and that is set when initial setting of the third initial setting area has been completed~~,~~; and

an n-th flag that is cleared by an input of any of the first reset signal through the n-th reset signal and that is set when initial setting of the n-th initial setting area has been completed, wherein: ~~when any one of the first through n-th reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first through n-th initial setting areas.~~

the method ~~comprising the steps of~~comprises:

clearing the first flag to the n-th flag ~~if~~ when the first reset signal is ~~received~~ input, clearing the ~~first and~~ second ~~flags~~ flag to the n-th flag ~~if~~ when the second reset signal is ~~received~~ input, clearing the ~~first through~~ third ~~flags~~ flag to n-th flag ~~if~~ when the third reset signal is ~~received~~ input, and clearing the ~~first through~~ n-th ~~flags~~ flag ~~if~~ when the n-th reset signal is ~~received~~ input;

~~checking which flag/s has/have been cleared out of the first through n-th flags;~~

~~initializing initial setting area/s corresponding to the cleared flag/s out of the first through n-th areas, and~~

when the first signal is input, initializing the first signal initial setting area after confirming that the first flag is cleared, initializing the second initial setting area after confirming that the first flag is set and the second flag is cleared, initializing the third signal initial setting area after confirming that the first and second flags are set and the third flag is cleared, and

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initializing the n-th initial setting area after confirming that the first flag through an (n-1)-th flag are set and the n-th flag is cleared;

when the second signal is input, initializing the second initial setting area after confirming that the first flag is set and the second flag is cleared without clearing the first flag, initializing the third signal initial setting area after confirming that the first and second flags are set and the third flag is cleared, and initializing the n-th initial setting area after confirming that the first through (n-1)-th flags are set and the n-th flag is cleared;

when the third signal is input, initializing the third initial setting area after confirming that the first and second flags are set and the third flag is cleared without clearing the first and second flags, and initializing the n-th initial setting area after confirming that the first through (n-1)-th flags are set and the n-th flag is cleared;

when the n-th reset signal is input, initializing the n-th initial setting area after confirming that the first through (n-1)-th flags are set and the n-th flag is cleared without clearing the first through (n-1)-th flags; and

~~setting flag/s corresponding to the initial setting area/s which has/have been initialized out of the first through n-th areas~~

setting each of the first flag to the n-th flag corresponding to each of the first initial setting area to the n-th setting area which is initialized.

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